THIN LEADLESS PLASTIC CHIP CARRIER

FIELD OF THE INVENTION

[0001] The present invention relates in general to integrated circuit packaging, and more particularly to a process for fabricating a leadless plastic chip carrier with a unique, low profile die attach pad.

BACKGROUND OF THE INVENTION

According to well known prior art IC (integrated circuit) packaging methodologies, semiconductor dice are singulated and mounted using epoxy or other conventional means onto respective die attach pads (attach paddles) of a leadframe strip. Traditional QFP (Quad Flat Pack) packages incorporate inner leads which function as lands for wire bonding the semiconductor die bond pads. These inner leads typically require mold locking features to ensure proper positioning of the leadframe strip during subsequent molding to encapsulate the package. The inner leads terminate in outer leads that are bent down to contact a mother board, thereby limiting the packaging density of such prior art devices.

[0002] In order to overcome these and other disadvantages of the prior art, the Applicants previously developed a Leadless Plastic Chip Carrier (LPCC). According to Applicants' LPCC methodology, a leadframe strip is provided for supporting several hundred devices. Singulated IC dice are placed on the strip die attach pads using conventional die mount and epoxy techniques. After curing of the epoxy, the dice are wire bonded to the peripheral internal leads by gold (Au), copper (Cu), aluminum (Al) or doped aluminum wire bonding. The leadframe strip is then molded in plastic or resin using a modified mold wherein the bottom cavity is a flat plate. In the resulting molded package, the die pad and leadframe inner leads are exposed. By exposing the bottom of the die attach pad, mold delamination at the bottom of the die pad is eliminated, thereby increasing the moisture sensitivity performance. Also, thermal performance of the IC package is improved by providing a direct thermal path from the exposed die attach pad to the motherboard. By exposing the leadframe inner leads, the requirement for mold locking features is eliminated and no external lead standoff is necessary, thereby increasing

device density and reducing package thickness over prior art methodologies. The exposed inner leadframe leads function as solder pads for motherboard assembly such that less gold wire bonding is required as compared to prior art methodologies, thereby improving electrical performance in terms of board level parasitics and enhancing package design flexibility over prior art packages (i.e. custom trim tools and form tools are not required). These and several other advantages of Applicants' own prior art LPCC process are discussed in Applicants' United States patent no. 6,229,200, the contents of which are incorporated herein by reference.

[0003] According to Applicants' U.S. patent no. 6,498,099, the contents of which are incorporated herein by reference, an etch back process is provided for the improved manufacture of the LPCC IC package. In Applicant's co-pending U.S. application serial no. 09/802,678, Entitled Leadless Plastic Chip Carrier With Etch Back Pad Singulation, filed March 9, 2001, the contents of which are incorporated herein by reference, the etch-back LPCC process of Applicants' United States patent no. 6,498,099 is modified to provide additional design features. The leadframe strip is selectively covered with a thin layer photo-resist mask in predetermined areas. Following the application of the mask, an etch-barrier is deposited as the first layer of the contact pads and die attach pad, followed by several layers of metals which can include for example, Ni, Cu, Ni, Au, and Ag. This method of formation of the contact pads allows plating of the pads in a columnar shape and into a "mushroom cap" or rivet-shape as it flows over the photoresist mask. The shaped contact pads are thereby locked in the mold body, providing superior board mount reliability. Similarly, the die attach pad can be formed in an interlocking shape for improved alignment with the die. The photo-resist mask is then rinsed away and the semiconductor die is mounted to the die attach pad. This is followed by gold wire bonding between the semiconductor die and the peripheral contact pads and then molding as described in Applicant's United States patent no. 6,229,200. The leadframe is then subjected to full immersion in an alkaline etchant that exposes a lower surface of an array of the contact pads, a power ring and the die attach pad, followed by singulation of the individual unit from the full leadframe array strip. This process includes the deposition or plating of a plurality of layers of metal to form a robust three-dimensional construction of contact pads and the die attach pad.

[0004] Still further improvements in high performance integrated circuit (IC) packages are driven by industry demands for increased thermal and electrical performance, decreased size and cost of manufacture.

[0005] For particular applications, multiple semiconductor die packages are used. This

requires additional space and large molds to accommodate increased package size due to stacking of semiconductor dice. Demand exists for reduced profile IC packages.

SUMMARY OF THE INVENTION

[0006] In one aspect of the present invention, a leadless plastic chip carrier is fabricated by selectively etching a leadframe strip to reduce a thickness of the strip at a portion thereof. Selectively masking the surface of the leadframe strip using a mask, follows selectively etching, to provide exposed areas of the surface at the portion and contact pad areas on leadframe the strip. At least one layer of metal is deposited on the exposed areas to define a die attach pad on the portion of the leadframe strip with reduced thickness and to define contact pads on the surface of the strip. At least one semiconductor die is mounted to the die attach pad, followed by wire bonding the at least one semiconductor die to ones of the contact pads. The at least one semiconductor die, the wire bonds, and the contact pads are covered with an overmold material and the leadframe strip is etched to thereby remove the leadframe strip. The leadless plastic chip carrier is singulated from the leadframe strip.

[0007] In another aspect, a process for fabricating a leadless plastic chip carrier includes selectively etching a leadframe strip to reduce a thickness of the strip at a portion thereof, selectively masking the surface of the leadframe strip using a mask to provide exposed areas of the surface at the portion and contact pad areas on the strip, depositing a plurality of layers of metal on the exposed areas to define a die attach pad on the portion of the strip with reduced thickness and to define contact pads on the surface of the strip, masking the die attach pad after depositing the at least one layer, depositing at least one further layer of metal on the at least one layer of metal at the contact pads thereby further defining the contact pads, stripping the mask from the die attach pad and the mask from the surface of the leadframe strip, mounting at least one semiconductor die to the die attach pad, wire bonding the at least one semiconductor die to ones of the contact pads, covering the at least one semiconductor die, the wire bonds, and the contact pads with an overmold material, etching the leadframe strip to thereby remove the leadframe strip, and singulating the leadless plastic chip carrier from the leadframe strip.

[0008] In yet another aspect, a leadless plastic chip carrier is provided. The leadless plastic chip carrier includes a die attach pad, at least one semiconductor die mounted on the die attach

pad, a plurality of contact pads circumscribing the die attach pad, a plurality of wire bonds connecting the at least one semiconductor die and various ones of the contact pads, and an overmold covering the semiconductor die and the contact pads, wherein the die attach pad is offset from the contact pads such that the die attach pad protrudes from the molding compound.

[0009] Advantageously, a thin package profile is possible as the die attach pad is offset from the contact pads and protrudes from the molding compound. Because the die attach pad is offset from the contact pads, the semiconductor die sits in a pocket on the die attach pad. Thus, the length of the wire bonds to the contact pads, to the power ring and to the die attach pad (ground) is reduced. This results in lower electrical impedance and permits operation of the package at higher frequencies.

[0010] Also, because the die attach pad is offset and protrudes from the molding compound, more space is provided within the package to accommodate several semiconductor dice stacked on top of each other, without significantly increasing the package size over standard, single semiconductor die packages.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The invention will be better understood with reference to the drawings and the following description in which like numerals denote like parts, and in which:

[0012] Figures 1A to 1L show processing steps for manufacturing a Leadless Plastic Chip Carrier (LPCC) according to one embodiment of the present invention;

[0013] Figure 2 is a bottom view of the LPCC manufactured according to the processing steps of Figures 1A to 1L; and

[0014] Figures 3A to 3L show processing steps for manufacturing a Leadless Plastic Chip Carrier according to another embodiment of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

[0015] Reference is first made to Figure 1L, to describe a Leadless Plastic Chip Carrier

(LPCC) indicated generally by the numeral 20. The leadless plastic chip carrier 20 includes a die attach pad 22 and a semiconductor die 24 mounted on the die attach pad 22. A plurality of contact pads 26 circumscribe the die attach pad 22 and a plurality of wire bonds 28 connect the semiconductor die 24 and various ones of the contact pads 26. An overmold 30 covers the semiconductor die 24 and the contact pads 26, wherein the die attach pad 22 is offset from the contact pads 26 such that the die attach pad 22 protrudes from the molding compound 30.

[0016] A process for fabricating the LPCC 20 will now be better described with reference to Figures 1A to 1L, which show processing steps for fabricating the LPCC 20 according to an embodiment of the present invention. Referring to Figure 1A, an elevation view is provided of a Cu (copper) panel substrate which forms the raw material of the leadframe strip 32. As discussed in greater detail in Applicant's United States Patent No. 6,229,200, issued May 8, 2001, the leadframe strip 32 is divided into a plurality of sections, each of which incorporates a plurality of leadframe units in an array (e.g. 3x3 array, 5x5 array, etc.). Only one such unit is depicted in the elevation view of Figure 1A, portions of adjacent units being represented by stippled lines. For the purpose of simplicity, the following description generally refers to a single unit of the leadframe strip 32. It will be understood, however, that the present description is not limited to a single unit, but relates to the plurality of leadframe units in the array.

[0017] Referring to Figure 1B, an upper surface of the leadframe strip 32 is coated with a layer of photo-imageable mask 34, such as a photo-imageable epoxy.

[0018] Next, the layer of photo-imageable etch-resist mask 34 is imaged with a photo-tool. This is accomplished by exposure of the photo-imageable mask 34 to ultraviolet light masked by the photo-tool and subsequent developing of the solder-mask to result in the configuration shown in Figure 1C. The photo-imageable mask 34 is thereby patterned to provide a pit in which the upper surface of the Cu substrate (leadframe strip 32) is exposed. Thus, the leadframe strip 32 is selectively masked with the photo-imageable mask 34.

[0019] The leadframe strip 32 is then etched on a top surface thereof and, following etching, the photo-imageable mask 34 is stripped away using conventional means. The resulting leadframe strip 32 includes a portion with reduced thickness where the leadframe strip 32 is selectively etched (Figure 1D).

[0020] Next, a plating mask 36 is added to the upper surface of the leadframe strip 32 (Figure 1E). As will be appreciated, the plating mask 36 is a photo-imageable plating mask 36

and is applied to the entire top surface of the leadframe strip 32. The photo-imageable plating mask 36 is then imaged with a photo-tool by exposure to ultraviolet light masked by the photo-tool. The photo-imageable plating mask is then developed to provide the pattern with exposed areas of the leadframe strip, as shown in Figure 1E.

[0021] As shown in Figure 1F, layers of metals are deposited on the upper surface of the exposed leadframe strip 32 to form the die attach pad 22 and portions of a ground ring 38, a power ring 40 and the contact pads 26. Different deposition options are provided.

[0022] According to option A, an etch barrier of Au (gold of, for example, 20 microinches) is provided over the Cu substrate, followed by a layer of Ni (nickel of, for example, 40 microinches), and then a layer of Cu (for example, 3-4 mils). According to option B, an etch barrier of Ag (silver) is followed by a layer of Cu. According to option C, an etch barrier of Pd (palladium) is followed by a layer of Ni and then Cu.

[0023] Referring now to Figure 1G, a second plating mask 42 is added to cover the die attach pad 22. As with the first plating mask 36, the second plating mask 42 is a photo-imageable plating mask 42 and is selectively applied to the die attach pad by adding the second plating mask 42, imaging with a photo-tool and developing to provide the mask shown in Figure 1G. Thus, the die attach pad 22 is masked from further metal plating.

[0024] After the second plating mask 42 is added, final layers of metal are deposited on the portions of the a ground ring 38, a power ring 40 and the contact pads 26. Different deposition options are provided, depending on the deposition option chosen in Figure 1F. A layer of Ni and a layer of Au are applied to the metal layers of option A. A layer of Ag is applied to the metal layers of option B. A layer of Ni and a layer of Pd are applied to the metal layers of option C. The final layers thereby complete the ground ring 38, power ring 40 and contact pads 26. After deposition of the final layers, the plating masks 36, 42 are stripped away, resulting in the configuration shown in Figure 1H.

[0025] Referring now to Figure 1I, the singulated semiconductor die 24 is conventionally mounted via epoxy, to the die attach pad 22 and the epoxy is cured. Other suitable mounting techniques are possible. Gold wires are then bonded between the semiconductor die 24 and the ground ring 38, between the semiconductor die 24 and the power ring 40, and between the semiconductor die 24 and ones of the contact pads 26. The leadframe strip 32 is then molded in a modified mold with a bottom cavity being a flat plate, and subsequently cured, as discussed

in Applicants' issued United States Patent No. 6,229,200.

[0026] The leadframe 32 is then subjected to a final alkaline etch that fully etches away the copper leadframe 32 and exposes the die attach pad 22, the ground ring 38, the power ring 40 and the contact pads 26 (Figure 1J). Clearly the ground ring 38 is continuous with the die attach pad 22. As shown in Figure 1J, the plane that the die attach pad 22 lies on, is offset (vertically in the Figure) from the plane that the power ring 40 and contact pads 26 lie on. Thus, the die attach pad 22 protrudes from a remainder of the components.

[0027] Next, a plurality of solder balls 44, commonly referred to as solder bumps, are placed on the exposed surfaces of the contact pads 26. The solder balls 44 are placed using known pick and place and reflow techniques (Figure 1K)

[0028] Singulation of the individual LPCC 20 is then performed either by saw singulation or by die punching, resulting in the package shown in Figure 1L. A bottom view of the package of Figure 1L is shown in Figure 2.

[0029] Referring now to Figure 3A to 3L, processing steps for fabricating a LPCC according to another embodiment of the present invention, are shown. The processing steps shown in figures 3A to 3H are similar to the processing steps described above with reference to Figures 1A to 1H and therefore need not be further described herein.

[0030] In Figure 3I, however, rather than mounting a single semiconductor die 24, as shown in Figure 1I and described above, a plurality of semiconductor dice 24a, 24b, 24c are mounted in a stacked arrangement, one on top of the other. To mount the semiconductor dice 24a, 24b, 24c, the first semiconductor die 24a is conventionally mounted via epoxy to the die attach pad 22. Next, gold wires are bonded between the semiconductor die 24a and ones of the ground ring 38, the power ring 40 and the contact pads 26. The second semiconductor die 24b is then mounted via epoxy to the first semiconductor die 24a. Next, gold wires are bonded between the semiconductor die 24b and ones of the ground ring 38, the power ring 40 and the contact pads 26. Finally, the third semiconductor die 24c is mounted via epoxy to the second semiconductor die 24b and gold wires are bonded between the semiconductor die 24c and ones of the ground ring 38, the power ring 40 and the contact pads 26. Thus, the semiconductor dice 24a, 24b are separated by a layer of epoxy. Similarly, the semiconductor dice 24b, 24c are separated by a layer of epoxy.

[0031] The leadframe strip 32 is then molded in a modified mold with a bottom cavity being

a flat plate, and subsequently cured, as discussed above.

[0032] Figures 3J to 3L are similar to Figures 1J to 1L and therefore are not further described herein.

[0033] Specific embodiments of the present invention have been shown and described herein. However, modifications and variations may occur to those skilled in the art. For example, rather than wire bonding between mounting of semiconductor dice 24a, 24b and 24c, the semiconductor dice 24a, 24b and 24c can be mounted in a stack followed by subsequent wire bonding in the case that the semiconductor die 24a is larger than the semiconductor dice 24b and 24c and the semiconductor die 24b is larger than the semiconductor die 24c. Other modifications and variations are possible. All such modifications and variations are believed to be within the sphere and scope of the present invention.